ABSTRACT OF THE DISCLOSURE

OCV coefficients in a path being an analysis target according to the number of gate stages are calculated in a coefficient arithmetically operating unit by canceling off a variation in delay in each gate in accordance with the number of gate stages in the target path, and timing analysis of the target path is performed in a timing analysis unit by using the OCV coefficient with the number of gate stages being considered, whereby a variation degree in the entire path is reduced in accordance with the number of gate stages in the target path, thus making it possible to carry out accurate timing analysis in consideration of the variation in a chip of a semiconductor integrated circuit.